# Ultralow Drift Op Amp

# AD707

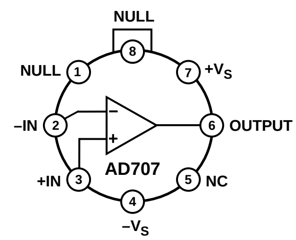
## FEATURES

**Very High DC Precision**
**15 μV max Offset Voltage**
**0.1 μV/°C max Offset Voltage Drift**
**0.35 μV p-p max Voltage Noise (0.1 Hz to 10 Hz)**
**8 V/μV min Open-Loop Gain**
**130 dB min CMRR**
**120 dB min PSRR**
**1 nA max Input Bias Current**

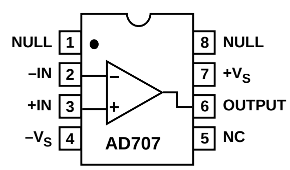
**AC Performance**
**0.3 V/μs Slew Rate**
**0.9 MHz Closed-Loop Bandwidth**
**Dual Version: AD708**
**Available in Tape and Reel in Accordance with EIA-481A Standard**

## CONNECTION DIAGRAMS

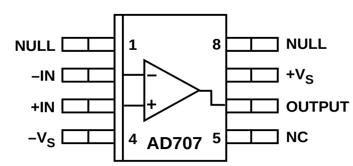
**TO-99 (H) Package**




**Plastic (N) and Cerdip (Q) Packages**




**SOIC (R) Package**




## PRODUCT DESCRIPTION

The AD707 is a low cost, high precision op amp with state-of-the-art performance that makes it ideal for a wide range of precision applications. The offset voltage spec of less than 15 μV is the best available in a bipolar op amp, and maximum input offset current is 1.0 nA. The top grade is the first bipolar monolithic op amp to offer a maximum offset voltage drift of 0.1 μV/°C, and offset current drift and input bias current drift are both specified at 25 pA/°C maximum.

The AD707's open-loop gain is 8 V/μV minimum over the full ±10 V output range when driving a 1 kΩ load. Maximum input voltage noise is 350 nV p-p (0.1 Hz to 10 Hz). CMRR and PSRR are 130 dB and 120 dB minimum, respectively.

The AD707 is available in versions specified over commercial, industrial and military temperature ranges. It is offered in 8-pin plastic mini-DIP, small outline (SOIC), hermetic cerdip and hermetic TO-99 metal can packages. Chips, MIL-STD-883B, Rev. C, and tape & reel parts are also available.

## APPLICATION HIGHLIGHTS

1. The AD707's 13 V/μV typical open-loop gain and 140 dB typical common-mode rejection ratio make it ideal for precision instrumentation applications.
2. The precision of the AD707 makes tighter error budgets possible at a lower cost.
3. The low offset voltage drift and low noise of the AD707 allow the designer to amplify very small signals without sacrificing overall system performance.
4. The AD707 can be used where chopper amplifiers are required, but without the inherent noise and application problems.
5. The AD707 is an improved pin-for-pin replacement for the LT1001.

REV. B



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# AD707–SPECIFICATIONS (@ +25°C and ±15 V, unless otherwise noted)

| | Conditions | AD707J/A Min | Typ | Max | AD707K/B Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| INPUT OFFSET VOLTAGE | | | | | | | | |
| Initial | | | 30 | **90** | | 10 | **25** | μV |
| vs. Temperature | | | 0.3 | 1.0 | | 0.1 | **0.3** | μV/°C |
| | $T_{MIN}$ to $T_{MAX}$ | | 50 | 100 | | 15 | **45** | μV |
| Long-Term Stability | | | 0.3 | | | 0.3 | | μV/month |
| Adjustment Range | R2 = 20 kΩ (Figure 19) | | ±4 | | | ±4 | | mV |
| INPUT BIAS CURRENT | | | 1.0 | 2.5 | | 0.5 | 2.0 | nA |
| | $T_{MIN}$ to $T_{MAX}$ | | 2.0 | 4.0 | | 1.5 | 4.0 | nA |
| Average Drift | | | 15 | 40 | | 15 | 40/40/40 | pA/°C |
| OFFSET CURRENT | $V_{CM}$ = 0 V | | 0.5 | 2.0 | | 0.3 | **1.5** | nA |
| | $T_{MIN}$ to $T_{MAX}$ | | 2.0 | 4.0 | | 1.0 | **2.0** | nA |
| Average Drift | | | 2 | 40 | | 1 | 25/25/35 | pA/°C |
| INPUT VOLTAGE NOISE | 0.1 Hz to 10 Hz | | 0.23 | 0.6 | | 0.23 | 0.6 | μV p-p |
| | f = 10 Hz | | 10.3 | 28 | | 10.3 | 18 | nV/√Hz |
| | f = 100 Hz | | 10.0 | 13.0 | | 10.0 | 12 | nV/√Hz |
| | f = 1 kHz | | 9.6 | 11.0 | | 9.6 | 11.0 | nV/√Hz |
| INPUT CURRENT NOISE | 0.1 Hz to 10 Hz | | 14 | 35 | | 14 | 30 | pA p-p |
| | f = 10 Hz | | 0.32 | 0.9 | | 0.32 | 0.8 | pA/√Hz |
| | f = 100 Hz | | 0.14 | 0.27 | | 0.14 | 0.23 | pA/√Hz |
| | f = 1 kHz | | 0.12 | 0.18 | | 0.12 | 0.17 | pA/√Hz |
| COMMON-MODE REJECTION RATIO | $V_{CM}$ = ±13 V | **120** | 140 | | **130** | 140 | | dB |
| | $T_{MIN}$ to $T_{MAX}$ | 120 | 140 | | **120** | 140 | | dB |
| OPEN-LOOP GAIN | $V_O$ = ±10 V | | | | | | | |
| | $R_{LOAD}$ ≥ 2 kΩ | **3** | 13 | | **5** | 13 | | V/μV |
| | $T_{MIN}$ to $T_{MAX}$ | **3** | 13 | | 3 | 13 | | V/μV |
| POWER SUPPLY REJECTION RATIO | $V_S$ = ±3 V to ±18 V | **110** | 130 | | **115** | 130 | | dB |
| | $T_{MIN}$ to $T_{MAX}$ | 110 | 130 | | 110 | 130 | | dB |
| FREQUENCY RESPONSE | | | | | | | | |
| Closed-Loop Bandwidth | | 0.4 | 0.9 | | 0.4 | 0.9 | | MHz |
| Slew Rate | | 0.12 | 0.3 | | 0.12 | 0.3 | | V/μs |
| INPUT RESISTANCE | | | | | | | | |
| Differential | | 24 | 100 | | 45 | 200 | | MΩ |
| Common Mode | | | 200 | | | 300 | | GΩ |
| OUTPUT CHARACTERISTICS | | | | | | | | |
| Voltage | $R_{LOAD}$ ≥ 10 kΩ | **13.5** | 14 | | **13.5** | 14 | | ±V |
| | $R_{LOAD}$ ≥ 2 kΩ | **12.5** | 13.0 | | **12.5** | 13.0 | | ±V |
| | $R_{LOAD}$ ≥ 1 kΩ | **12.0** | 12.5 | | **12.0** | 12.5 | | ±V |
| | $R_{LOAD}$ ≥ 2 kΩ, $T_{MIN}$ to $T_{MAX}$ | 12.0 | 13.0 | | **12.0** | 13.0 | | ±V |
| OPEN-LOOP OUTPUT RESISTANCE | | | 60 | | | 60 | | Ω |
| POWER SUPPLY | | | | | | | | |
| Current, Quiescent | | | 2.5 | **3** | | 2.5 | **3** | mA |
| Power Consumption, No Load | $V_S$ = ±15 V | | 75 | **90** | | 75 | **90** | mW |
| | $V_S$ = ±3 V | | 7.5 | **9.0** | | 7.5 | **9.0** | mW |

NOTES

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS[1]

| | |
|---|---|
| Supply Voltage | ±22 V |
| Internal Power Dissipation[2] | 500 mW |
| Input Voltage | $\pm V_S$ |
| Output Short Circuit Duration | Indefinite |
| Differential Input Voltage | $+V_S$ and $-V_S$ |
| Storage Temperature Range (Q, H) | –65°C to +150°C |
| Storage Temperature Range (N, R) | –65°C to +125°C |
| Lead Temperature Range (Soldering 60 sec) | +300°C |

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

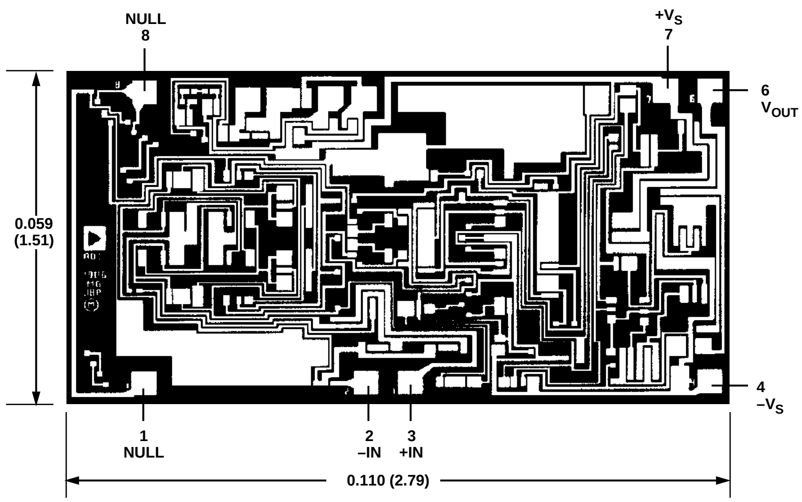
[2]8-pin plastic package: $\theta_{JA}$ = 165°C/Watt; 8-pin cerdip package: $\theta_{JA}$ = 110°C/Watt; 8-pin small outline package: $\theta_{JA}$ = 155°C/Watt; 8-pin header package: $\theta_{JA}$ = 200°C/Watt.

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD707AH | –40°C to +85°C | 8-Pin Metal Can | H-08A |
| AD707AQ | –40°C to +85°C | 8-Pin Ceramic DIP | Q-8 |
| AD707AR | –40°C to +85°C | 8-Pin Plastic SOIC | SO-8 |
| AD707AR-REEL | –40°C to +85°C | 8-Pin Plastic SOIC | SO-8 |
| AD707AR-REEL7 | –40°C to +85°C | 8-Pin Plastic SOIC | SO-8 |
| AD707BQ | –40°C to +85°C | 8-Pin Ceramic DIP | Q-8 |
| AD707JN | 0°C to +70°C | 8-Pin Plastic DIP | N-8 |
| AD707JR | 0°C to +70°C | 8-Pin Plastic SOIC | SO-8 |
| AD707JR-REEL | 0°C to +70°C | 8-Pin Plastic SOIC | SO-8 |
| AD707JR-REEL7 | 0°C to +70°C | 8-Pin Plastic SOIC | SO-8 |
| AD707KN | 0°C to +70°C | 8-Pin Plastic DIP | N-8 |
| AD707KR | 0°C to +70°C | 8-Pin Plastic SOIC | SO-8 |
| AD707KR-REEL | 0°C to +70°C | 8-Pin Plastic SOIC | SO-8 |
| AD707KR-REEL7 | 0°C to +70°C | 8-Pin Plastic SOIC | SO-8 |

## METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.




## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD707 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



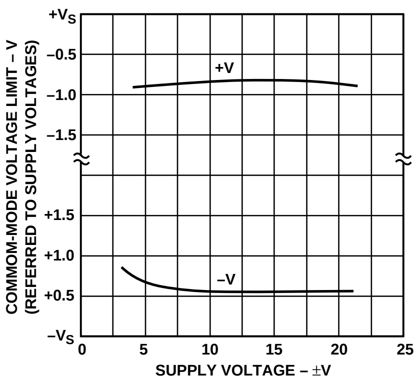



*Figure 1. Input Common-Mode Range vs. Supply Voltage*

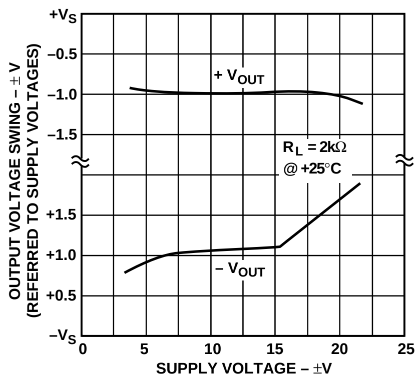



*Figure 2. Output Voltage Swing vs. Supply Voltage*

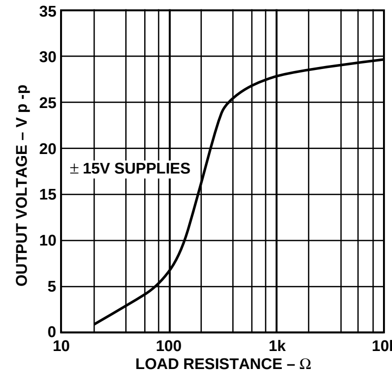



*Figure 3. Output Voltage Swing vs. Load Resistance*

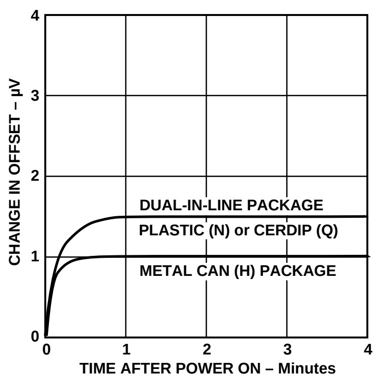



*Figure 4. Offset Voltage Warm-Up Drift*

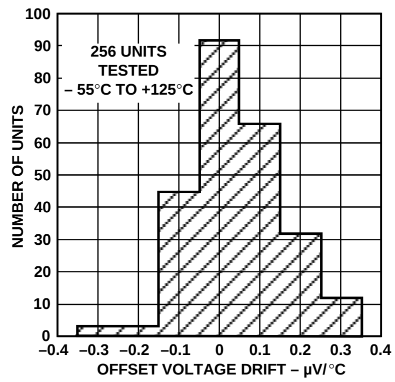



*Figure 5. Typical Distribution of Offset Voltage Drift*

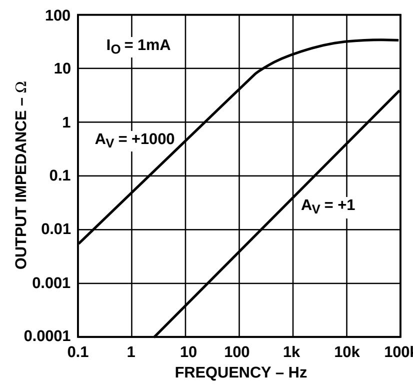



*Figure 6. Output Impedance vs. Frequency*

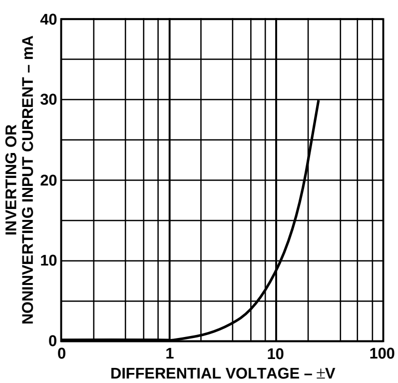



*Figure 7. Input Current vs. Differential Input Voltage*

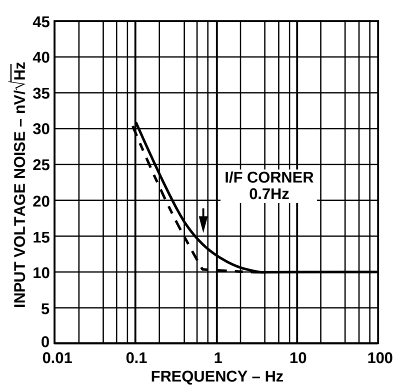



*Figure 8. Input Noise Spectral Density*

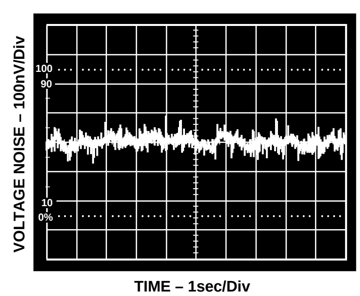



*Figure 9. 0.1 Hz to 10 Hz Voltage Noise*

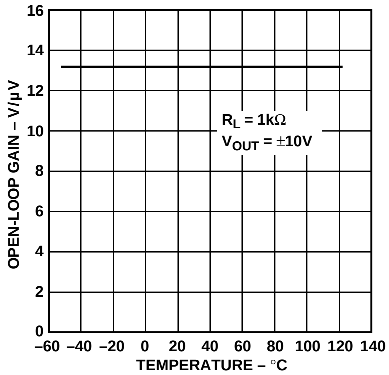



*Figure 10. Open-Loop Gain vs. Temperature*

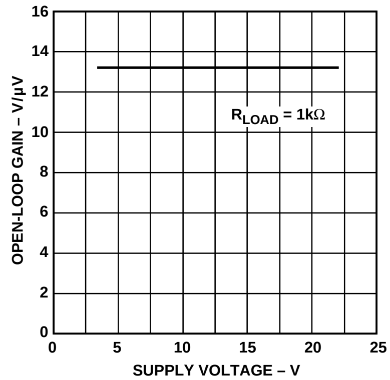



*Figure 11. Open-Loop Gain vs. Supply Voltage*

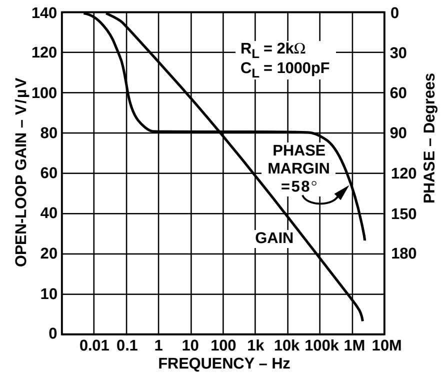



*Figure 12. Open-Loop Gain and Phase vs. Frequency*

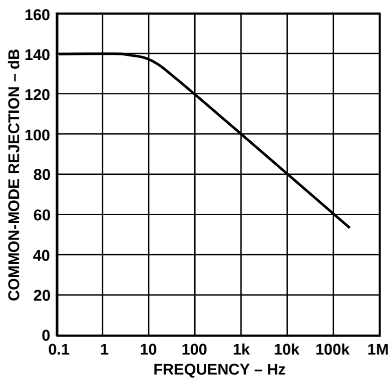



*Figure 13. Common-Mode Rejection vs. Frequency*

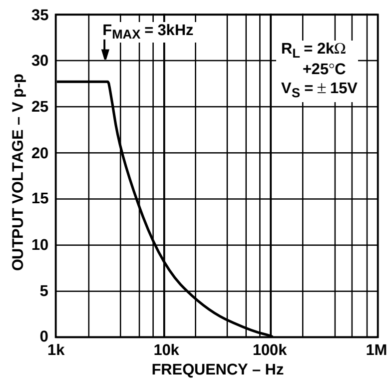



*Figure 14. Large Signal Frequency Response*

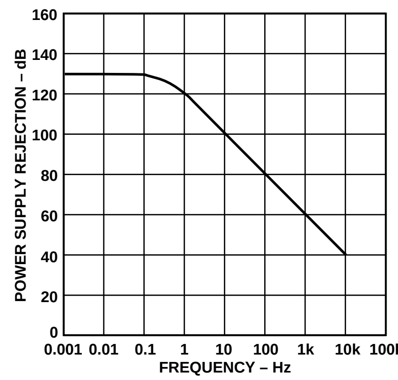



*Figure 15. Power Supply Rejection vs. Frequency*

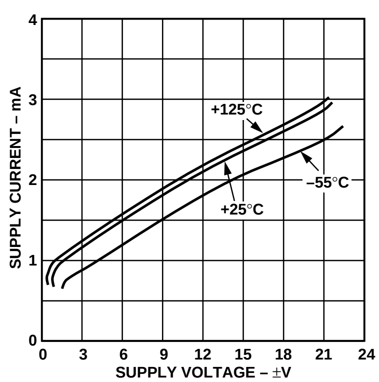



*Figure 16. Supply Current vs. Supply Voltage*

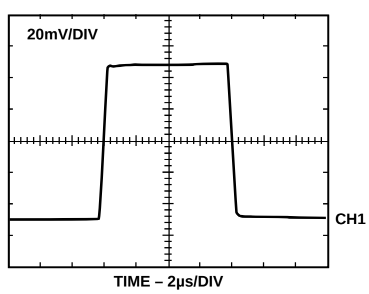



*Figure 17. Small Signal Transient Response; $A_V = +1$, $R_L = 2\ k\Omega$, $C_L = 50\ pF$*

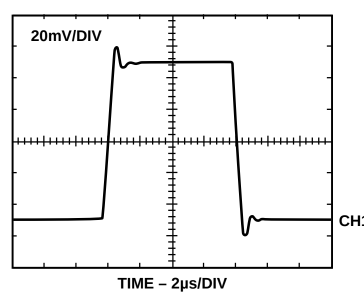



*Figure 18. Small Signal Transient Response; $A_V = +1$, $R_L = 2\ k\Omega$, $C_L = 1000\ pF$*

## OFFSET NULLING

The input offset voltage of the AD707 is the lowest available in a bipolar op amp, but if additional nulling is required, the circuit shown in Figure 19 offers a null range of 200 µV. For wider null capability, omit R1 and substitute a 20 kΩ potentiometer for R2.

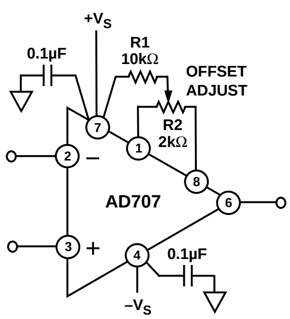



*Figure 19. External Offset Nulling and Power Supply Bypassing*

## GAIN LINEARITY INTO A 1 kΩ LOAD

The gain and gain linearity of the AD707 are the highest available among monolithic bipolar amplifiers. Unlike other dc precision amplifiers, the AD707 shows no degradation in gain or gain linearity when driving loads in excess of 1 kΩ over a ±10 V output swing. This means high gain accuracy is assured over the output range. Figure 20 shows the gain of the AD707, OP07, and the OP77 amplifiers when driving a 1 kΩ load.

The AD707 will drive 10 mA of output current with no significant effect on its gain or linearity.

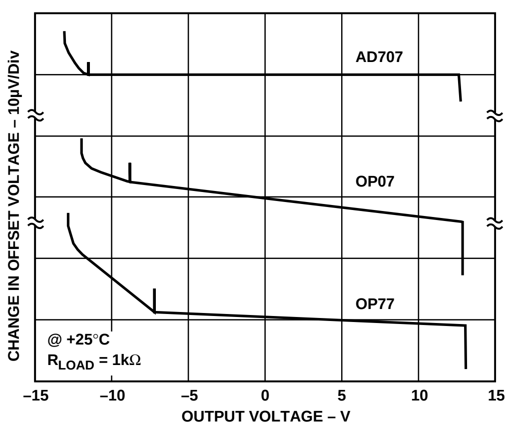



*Figure 20. Gain Linearity of the AD707 vs. Other DC Precision Op Amps*

## OPERATION WITH A GAIN OF 100

Demonstrating the outstanding dc precision of the AD707 in practical applications, Table I shows an error budget calculation for the gain of –100 configuration shown in Figure 21.

**Table I. Error Budget**

| Error Source | Maximum Error Contribution Av = 100 (C Grade) (Full Scale: $V_{OUT}$ = 10 V, $V_{IN}$ = 100 mV) | |
|---|---|---|
| $V_{OS}$ | 15 µV/100 mV | = 150 ppm |
| $I_{OS}$ | (100 Ω)(1 nA)/100 mV | = 1 ppm |
| Gain (2 kΩ Load) | (100 V/8 × $10^6$)100 mV | = 13 ppm |
| Noise | 0.35 µV/100 mV | = 4 ppm |
| $V_{OS}$ Drift | (0.1 V/°C)/100 mV | = 1 ppm/°C |
| | | = 168 ppm +1 ppm/°C |

Total Unadjusted Error

| | |
|---|---|
| @ +25°C | = 168 ppm > 12 Bits |
| @ –55°C to +125°C | = 268 ppm > 11 Bits |
| With Offset Calibrated Out | |
| @ +25°C | = 17 ppm > 15 Bits |
| @ –55°C to +125°C | = 117 ppm > 13 Bits |

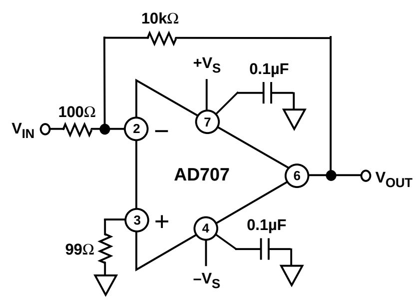



*Figure 21. Gain of –100 Configuration*

Although the initial offset voltage of the AD707 is very low, it is nonetheless the major contributor to system error. In cases requiring additional accuracy, the circuit shown in Figure 19 can be used to null out the initial offset voltage. This method will also cancel the effects of input offset current error. With the offsets nulled, the AD707C will add less than 17 ppm of error.

This error budget assumes no error in the resistor ratio and no errors from power supply variation (the 120 dB minimum PSRR of the AD707C makes this a good assumption). The external resistors can cause gain error from mismatch and drift over temperature.

## 18-BIT SETTLING TIME

Figure 22 shows the AD707 settling to within 80 µV of its final value for a 20 V output step in less than 100 µs (in the test configuration shown in Figure 23). To achieve settling to 18 bits, any amplifier specified to have a gain of 4 V/µV would appear to be good enough, however, this is not the case. In order to truly achieve 18-bit accuracy, the gain linearity must be better than 4 ppm.

The gain nonlinearity of the AD707 does not contribute to the error, and the gain itself only contributes 0.1 ppm. The gain error, along with the $V_{OS}$ and $V_{OS}$ drift errors do not comprise 1 LSB of error in an 18-bit system over the military temperature range. If calibration is used to null offset errors, the AD707 resolves up to 20 bits at +25°C.

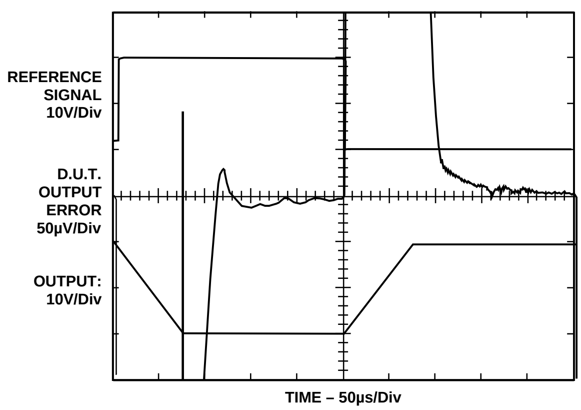



*Figure 22. 18-Bit Settling*

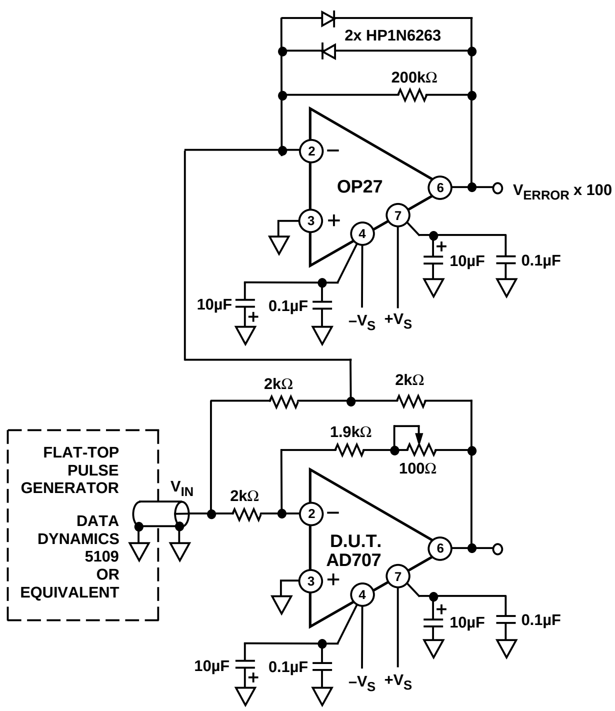



*Figure 23. Op Amp Settling Time Test Circuit*

## 140 dB CMRR INSTRUMENTATION AMPLIFIER

The extremely tight dc specifications of the AD707 enable the designer to build very high performance, high gain instrumentation amplifiers without having to select matched op amps for the crucial first stage. For the second stage, the lowest grade AD707 is ideally suited. The CMRR is typically the same as the high grade parts, but does not exact a premium for drift performance (which is less critical in the second stage). Figure 24 shows an example of the classic instrumentation amp. Figure 25 shows that the circuit has at least 140 dB of common-mode rejection for a ±10 V common-mode input at a gain of 1001 ($R_G$ = 20 Ω).

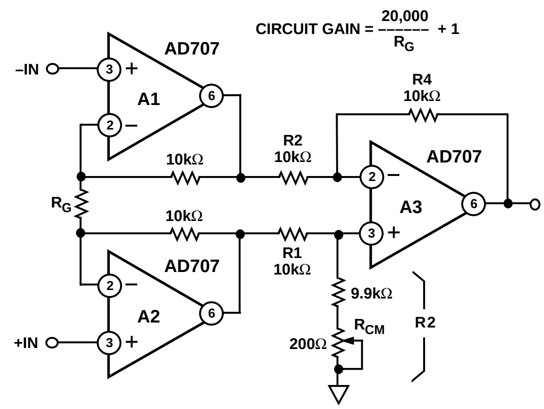



*Figure 24. A 3 Op Amp Instrumentation Amplifier*

High CMRR is obtained by first adjusting $R_{CM}$ until the output does not change as the input is swept through the full common-mode range. The value of $R_G$, should then be selected to achieve the desired gain. Matched resistors should be used for the output stage so that $R_{CM}$ is as small as possible. The smaller the value Of $R_{CM}$, the lower the noise introduced by potentiometer wiper vibrations. To maintain the CMRR at 140 dB over a 20°C range, the resistor ratios in the output stage, R1/R2 and R3/R4, must track each other better than 10 ppm/°C.

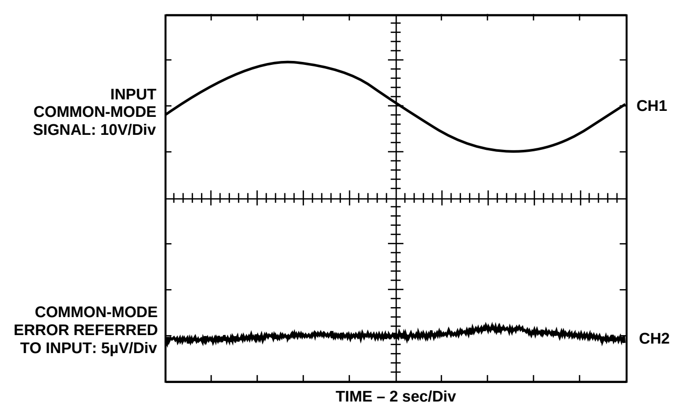



*Figure 25. Instrumentation Amplifier Common-Mode Rejection*

## PRECISION CURRENT TRANSMITTER

The AD707's excellent dc performance, especially the low offset voltage, low offset voltage drift and high CMRR, makes it possible to make a high precision voltage-controlled current transmitter using a variation of the Howland Current Source circuit (Figure 26). This circuit provides a bidirectional load current which is derived from a differential input voltage.

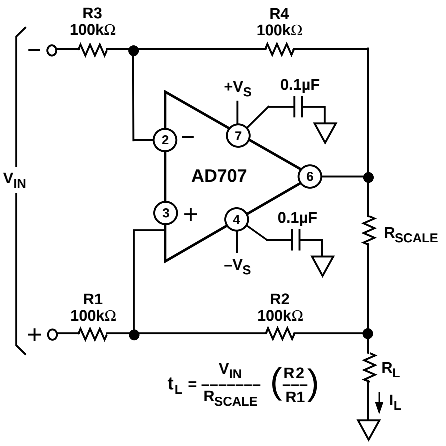



*Figure 26. Precision Current Source/Sink*

The performance and accuracy of this circuit will depend almost entirely on the tolerance and selection of the resistors. The scale resistor ($R_{SCALE}$) and the four feedback resistors directly affect the accuracy of the load current and should be chosen carefully or trimmed.

As an example of the accuracy achievable, assume $I_L$ must be 10 mA, and the available $V_{IN}$ is only 10 mV.

$R_{SCALE}$ = 10 mV/10 mA = 1 Ω

$I_{ERROR}$ due to the AD707C:

$$\text{Maximum } I_{ERROR} = 2(V_{OS})/R_{SCALE} + 2(V_{OS}\ \text{Drift})/R_{SCALE} + I_{OS}\ (100\ \text{k}/R_{SCALE})$$

$$= 2\ (15\ \mu V)/1\ \Omega + 2\ (0.1\ \mu V/°C)/1\ \Omega + 1\ nA\ (100\ k)/1\ \Omega\ (1.5\ nA\ @\ 125°C)$$

$$= 30\ \mu A + 0.2\ \mu A/°C + 100\ \mu A\ (150\ \mu A\ @\ 125°C)$$

$$= 130\ \mu A/10\ mA = 1.3\%\ @\ 25°C$$

$$= 180\ \mu A/10\ mA = 1.8\%\ @\ 125°C$$

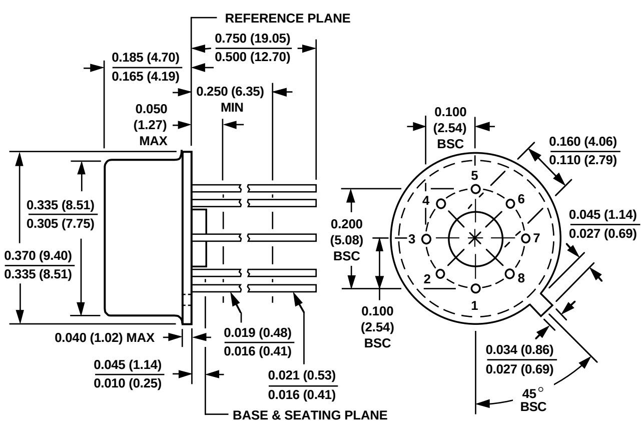
Low drift, high accuracy resistors are required to achieve high precision.

C1164a–2–12/95

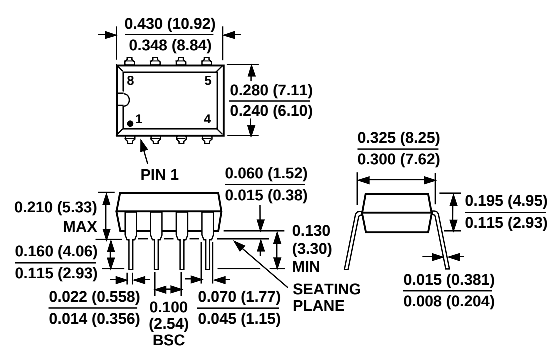
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

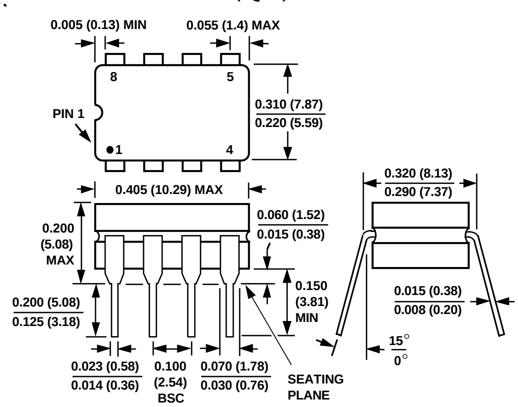
### 8-Pin Metal Can (H-08A)



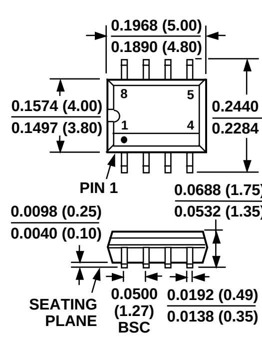

### 8-Pin Plastic DIP (N-8)

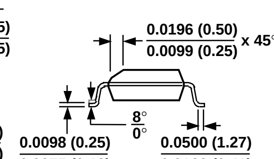



### 8-Pin Cerdip (Q-8)




### 8-Lead SOIC (SO-8)




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